G1N65R035TB

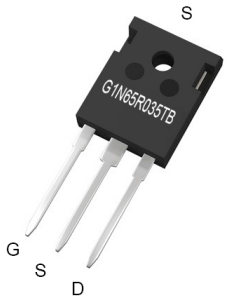
650V GaN FET

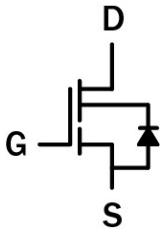
Preliminary Datasheet

1. Description

The G1N65 series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

TO-247
(top view)





Schematic Symbol

Features

- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_G and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Low Q_{RR} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

- Enable highest conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced thermal budget.
- Improved safety & reliability due to cooler operation temperature.

Applications

- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits.
- High-efficiency/High-frequency phase-shift, LLC or other soft-switching topologies.

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DS(PK)}$ (V) [a]	800
$R_{DS(ON)}$ (mΩ) typical [b]	35
Q_{OSS} (nC)	150
Q_G (nC)	22

[a] Duty<1%, spike duration <1μs, nonrepetitive
[b] Dynamic on-resistance

Part Number & Package Information		
Part #	Package	Package Base
G1N65R035TB	TO-247	Source

2. Maximum Ratings & Thermal Characteristics

Name	Parameter	Value
V_{DSS} (V)	Maximum drain-to-source voltage (T_j = -55°C to 150°C)	650
$V_{DSS(PK)}$ (V)	Maximum peak drain-to-source voltage [a]	800
V_{GSS}(V)	Maximum gate-to-source voltage	±20
P_D(W)	Maximum power dissipation (T_C=25°C)	156
I_{DS}(A)	Maximum continuous drain current (T_C=25°C)	46.5
	Maximum continuous drain current (T_C=100°C)	29.5
I_{DS}(Pulsed)(A)	Maximum pulse drain current (T_C=25°C) [b]	240
T_c (°C)	Case temperature	-55 to +150
T_j (°C)	Junction temperature	-55 to +150
T_s (°C)	Storage temperature	-55 to +150
T_{sold} (°C)	Soldering peak temperature [c]	260
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	0.8
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance	40

[a] Duty cycle<1%, spike duration <1μs, nonrepetitive

[b] Pulse width=10μs

[c] For 10 seconds, 1.6mm from the case

3. Device Characteristics

T_j=25℃ unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DSS}	Drain-to-source voltage	650	-	-	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS}=V_{GS}, I_D=1mA
$\Delta V_{GS(th)}/T_j$	Gate threshold voltage temperature coefficient	-	-6.5	-	mV/°C	V_{DS}=V_{GS}, I_D=1mA
$R_{DS(ON)}$	Drain-source on resistance [a]	-	35	41	mΩ	V_{GS}=10V, I_D=30A
			72	-	mΩ	V_{GS}=10V, I_D=30A, T_j=150°C
I_{DSS}	Off-state drain-to-source leakage current	-	3	30	μA	V_{DS}=650V, V_{GS}=0V
		-	20	-	μA	V_{DS}=650V, V_{GS}=0V, T_j=150°C
I_{GSS}	Gate-to-source leakage current	-	-	400	nA	V_{GS}=20V
		-	-	-400	nA	V_{GS}=-20V
C_{ISS}	Input capacitance	-	1500	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{OSS}	Output capacitance	-	147	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{RSS}	Reverse switching capacitance	-	5	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
$C_{O(ER)}$	Equivalent output capacitance (energy related)	-	220	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(TR)}$	Equivalent output capacitance (time related)	-	380	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
Q_G	Total gate charge	-	22	-	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=32A
Q_{GS}	Gate-source charge	-	8.4	-	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=32A
Q_{GD}	Gate-drain charge	-	6.6	-	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=32A
Q_{OSS}	Output charge	-	150	-	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(ON)}$	Turn-on delay time	-	60	-	ns	V_{DS}=400V, V_{GS}=0V to 12V, I_D=32A, R_G=30Ω, Z_{FB}=120 Ω at 100MHz
t_R	Rise time	-	10	-	ns	
$t_{D(OFF)}$	Turn-off delay time	-	94	-	ns	
t_F	Fall time	-	10	-	ns	

[a] Dynamic ON-resistance.

Reverse Device Characteristics, T_J=25℃ unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
I_S	Reverse current	-	-	29.5	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	-	1.8	-	V	V_{GS}=0V, I_S=32A
		-	1.3	-	V	V_{GS}=0V, I_S=16A
t_{RR}	Reverse recovery time	-	60	-	ns	I_S=32A, V_{DD}=400V, di/dt=1000A/μs
Q_{RR}	Reverse recovery charge	-	150	-	nC	
$(di/dt)_{RM}$	Reverse diode di/dt [b]	-	-	3200	A/μs	When body diode is used for free wheeling

[a] Includes dynamic R_{DS-ON} effect.
[b] di/dt is automatically satisfied with the recommended circuit in Section 6.

4. Typical Characteristics (T_C=25 ℃ unless specified)

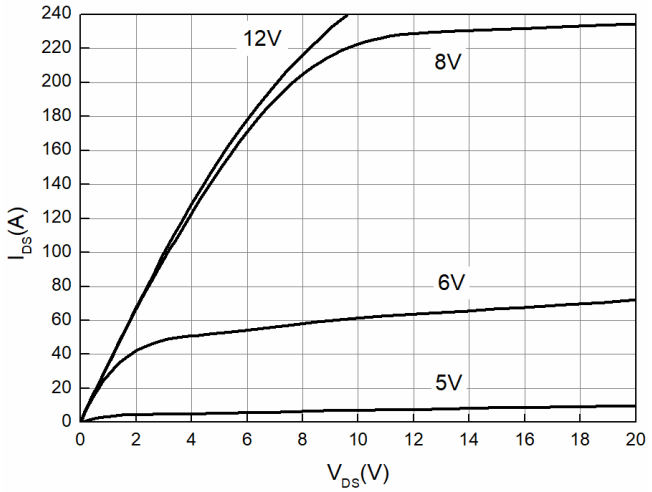


Figure 1. Typical Output Characteristics at T_j=25 ℃ (Parameter: V_{GS})

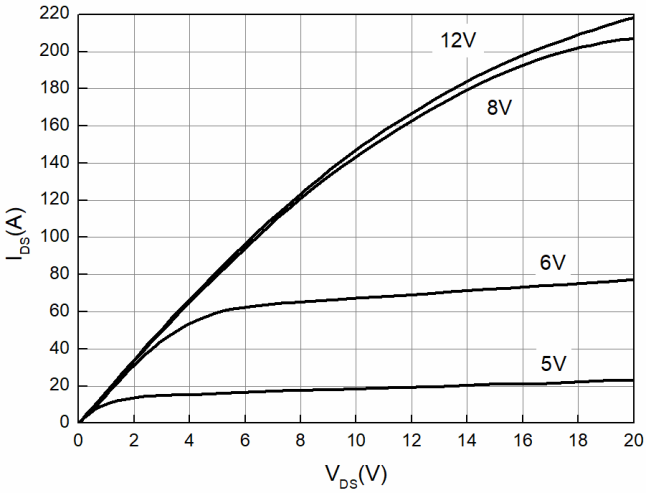


Figure 2. Typical Output Characteristics at T_j=150 ℃ (Parameter: V_{GS})

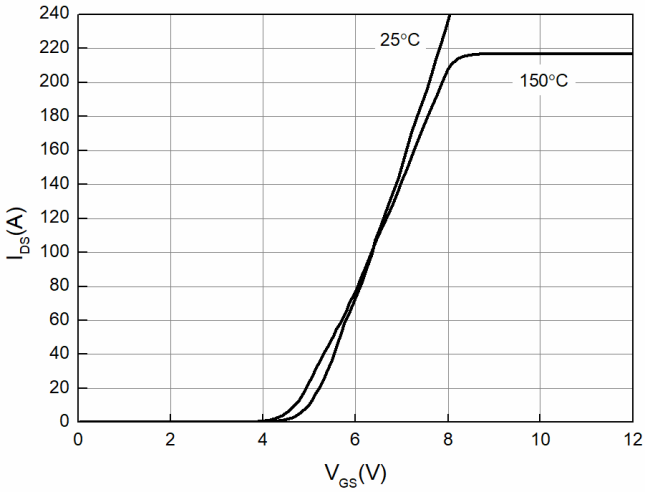


Figure 3. Typical Transfer Characteristics (V_{DS}=20V, parameter: T_j)

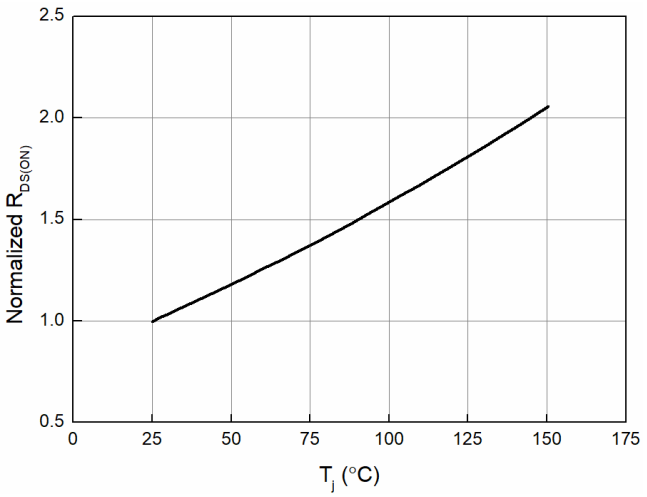


Figure 4. Normalized ON-resistance (I_D=30A, V_{GS}=8V)

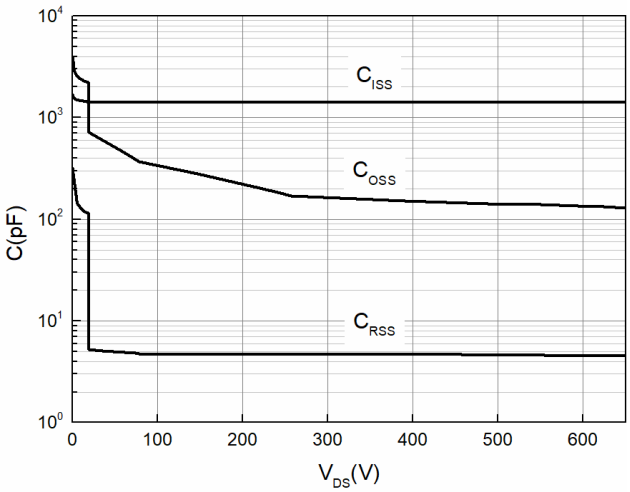


Figure 5. Typical Capacitance (V_{GS}=0V, f=1MHz)

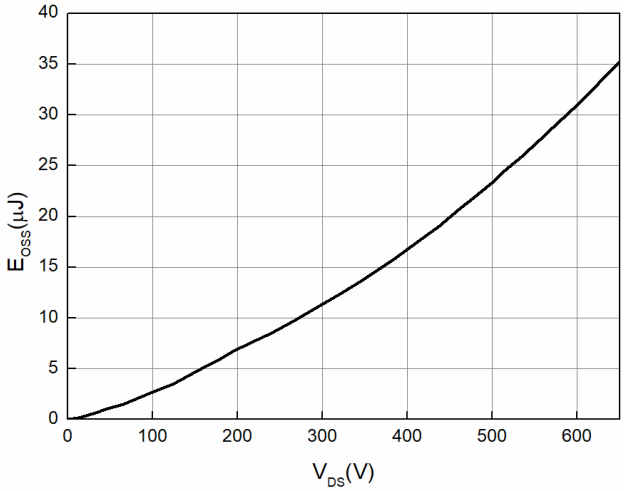


Figure 6. Typical C_{OSS} Stored Energy

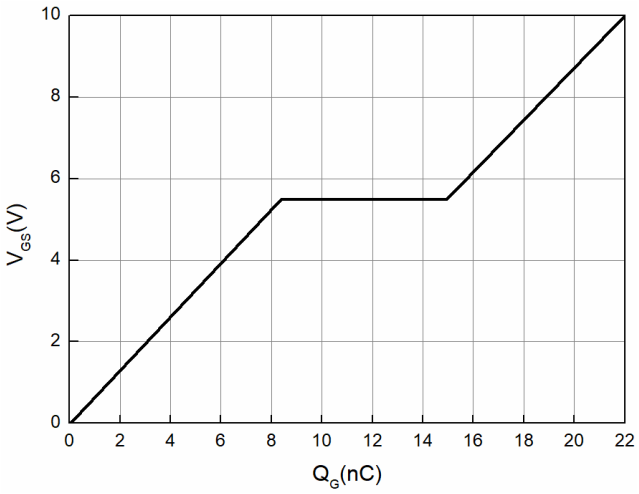


Figure 7. Typical Gate Charge (I_{DS}=32A, V_{DS}=400V)

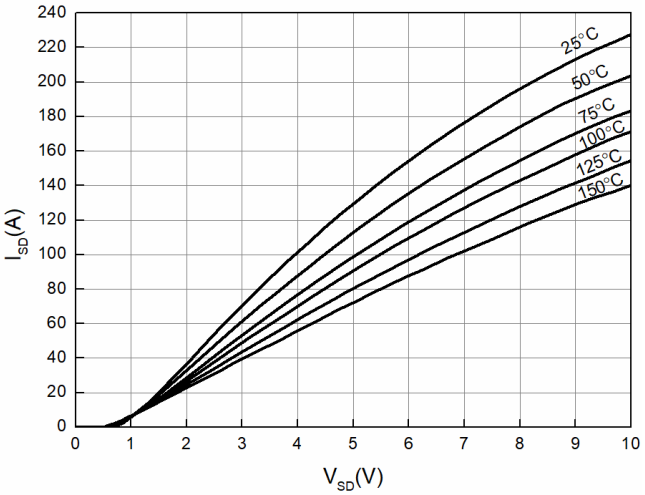


Figure 8. Reverse Conduction Characteristics (Parameter: T_j)

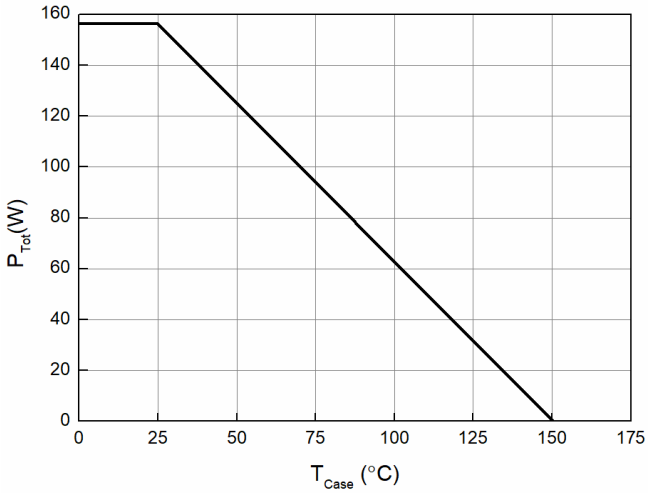


Figure 9. Power Dissipation

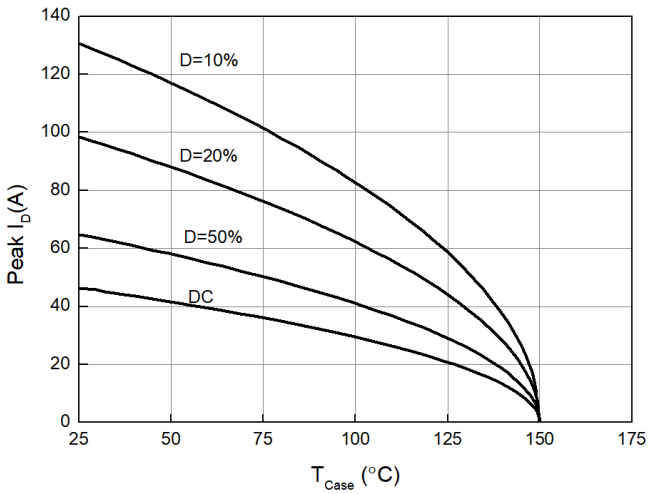


Figure 10. Current Derating (Pulse width: 10μs, V_{GS}: 10V)

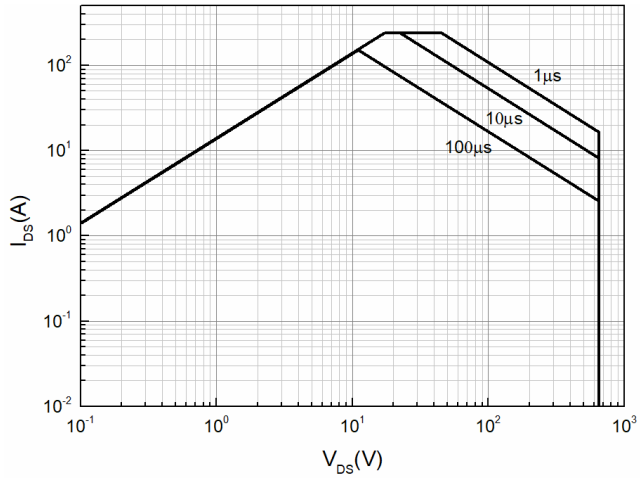


Figure 11. Safe Operating Area at T_C=25°C

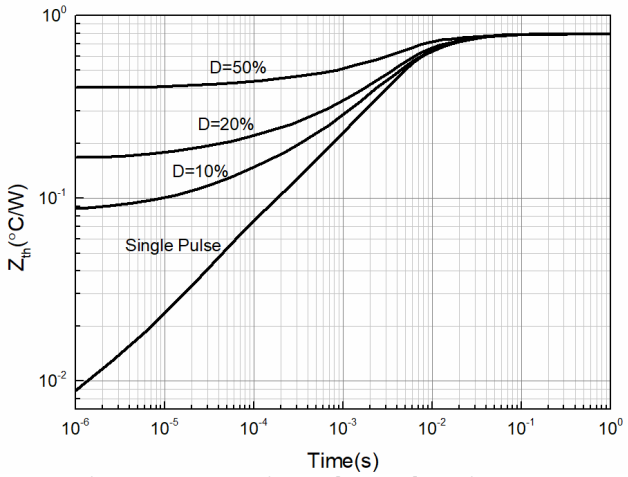


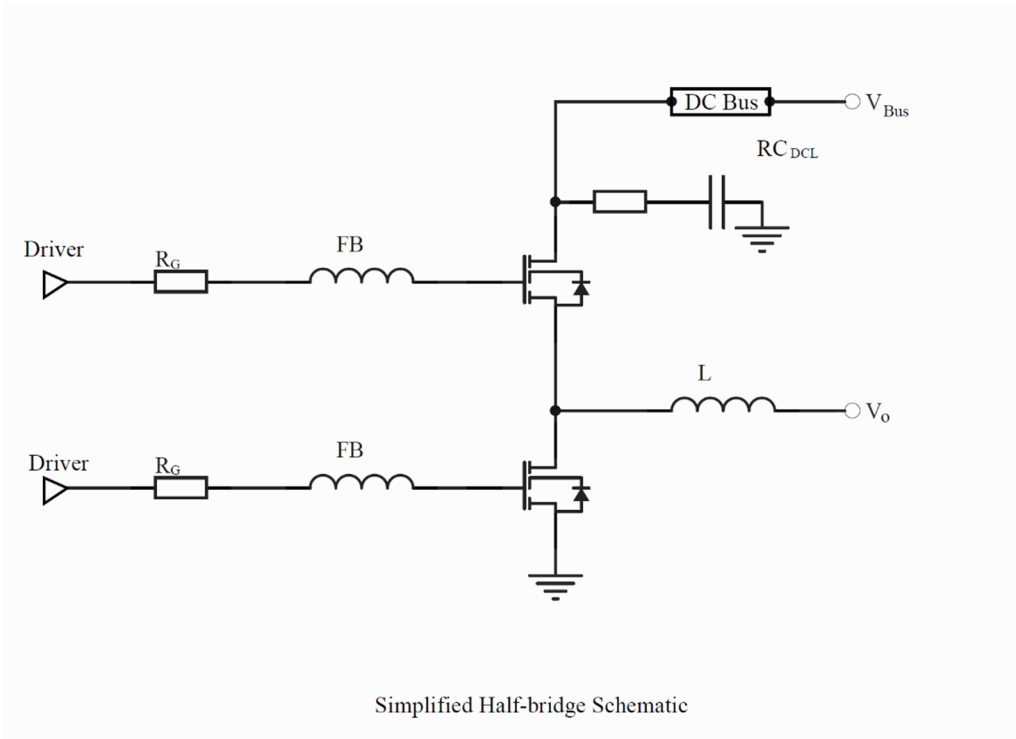
Figure 12. Transient Thermal Resistance

5. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate drives close to the GaN device and separate input traces from output traces	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor

6. Circuit Implementation



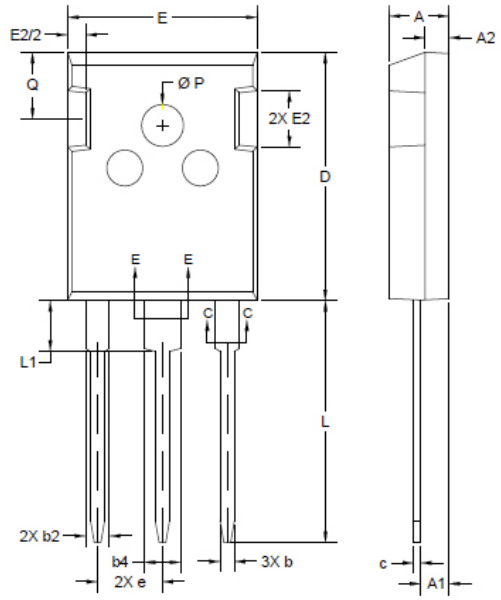
Simplified Half-bridge Schematic

Recommended gate drive: (0V, 12V) with R_G = 30 Ω [a)]

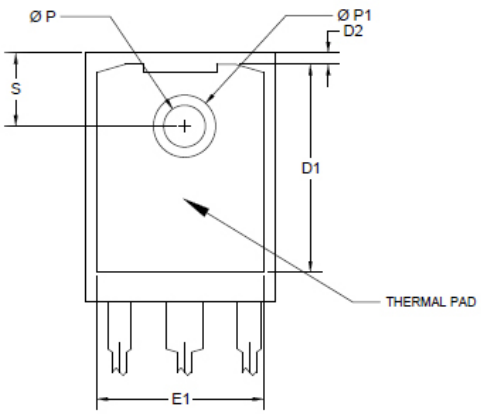
Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) [b)]
120-240Ω @ 100MHz	10-20nF + 3-5Ω

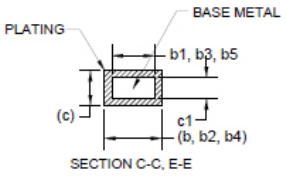
Notes:
[a)] For bridge topologies only. R_G could be smaller in single ended topologies.
[b)] RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitor(s) should be located away from the RC_{DCL}.

7. Package Dimensions



DIM	mm		
	Min.	Typ.	Max.
A	4.82	5.00	5.19
A1	2.20	2.39	2.57
A2	1.82	2.01	2.18
b	1.09	1.19	1.35
b1	1.09	-	1.30
b2	1.87	2.03	2.31
b3	1.87	-	2.27
b4	2.94	3.05	3.22
b5	2.94	-	3.18
c	0.50	0.58	0.68
c1	0.50	-	0.64
D	20.67	20.85	21.11
D1	17.20	0	17.63
D2	0.81	0	1.2
E	15.72	15.90	16.15
E1	13.79	-	14.25
E2	4.30	-	4.86
e	5.46 BSC	5.46 BSC	5.46 BSC
L	19.55	19.94	20.38
L1	3.93	4.11	4.48
ØP	3.50	3.61	3.69
ØP1	7.08	7.19	7.32
Q	5.41	-	5.85
S	6.15 BSC	6.15 BSC	6.15 BSC
TO-247 3L			
GaNext			
Date: 2020.12		Rev.01	





Notes:
1.Dimensions D & E do not include mold flash. Mold flash shall not exceed 0.127 MM per side. These dimensions are measured at the outermost extreme of the plastic body.

2. Thermal pad contour is optional within dimensions D1 & E1.

3. Lead finish uncontrolled in L1.

8. Revision History

Revision No.	Date	Description of Change(s)
Rev01	2020-12-15	First Edition